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Claims

[c1] A field effect transistor (FET) comprising:
a device channel;
a gate disposed above said device channel;
a doped extension at said each end of said thin channel, said doped extension being a source/drain extension; and
portions of a low resistance material layer disposed on said gate and on said source/drain extension, lateral extension contact said portions providing direct contact with said source/drain extension, gate said portions on said gate being separated from said lateral extension contact portions.

[c2] A FET as in claim 1, wherein each said source/drain extension has a lateral thickness of less than 100Å thick.

[c3] A FET as in claim 2, wherein said low resistance material layer is a silicide layer.

[c4] A FET as in claim 3, wherein said device channel is silicon and said source/drain extension is a doped silicon layer.

[c5] A FET as in claim 4, wherein said gate comprises polysilicon.

[c6] A FET as in claim 2, wherein said FET is a p-type FET (PFET).

[c7] A FET as in claim 2, wherein said FET is a n-type FET (NFET).

[c8] A FET as in claim 2, wherein said FET is one of a plurality of said FETs on a semiconductor substrate, ones of said plurality being p-type FETs (PFETs) and remaining ones being n-type FETs (NFETs).

[c9] A FET as in claim 8, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate.

[c10] A FET as in claim 8, wherein said semiconductor substrate is a bulk silicon substrate.

[c11] A FET as in claim 4, wherein said silicide forms a smooth silicide/silicon interface with said doped epi layer.

[c12] A FET as in claim 11, wherein smooth silicide/silicon interface has a roughness of less than 100Å.

[c13] A FET as in claim 4, wherein said source drain/extensions are laterally formed on an angled undercut following a silicon crystal (111) crystallographic plane.

[c14] A FET as in claim 2, wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi_2), cobalt ($CoSi_2$), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

[c15] A FET as in claim 14, wherein said silicide is selected from the group of metals consisting of WSi_2, NiSi and $CoSi_2$.

[c16] A FET as in claim 2, wherein said low resistance material layer comprises a metal selected from a group of metals consisting of tungsten, cobalt, nickel, titanium, platinum and Erbium.

[c17] An integrated circuit (IC) including a plurality of field effect transistors (FETs) disposed on a semiconductor substrate, each of said FETs comprising:
a device channel;
a gate disposed above said device channel;
a source/drain extension less than 100Å thick and disposed at said each end of said thin channel; and
a portion of a low resistance material layer forming a smooth interface with and directly contacting a corresponding said source/drain extension.

[c18] An IC as in claim 17, wherein said low resistance material layer is a silicide layer.

[c19] An IC as in claim 18, wherein each said device channel is silicon, each said gate is polysilicon and each source/drain extension is doped silicon.

[c20] An IC as in claim 19, wherein said plurality of FETs comprise a plurality of p-type FETs (PFETs) and a plurality of n-type FETs (NFETs) connected together in a circuit.

[c21] An IC as in claim 20, wherein said semiconductor substrate is a silicon on insulator (SOI) substrate.

[c22] An IC as in claim 20, wherein said semiconductor substrate is a bulk silicon substrate.

[c23] An IC as in claim 19, wherein smooth silicide/silicon interface has a roughness of less than 100Å, whereby said corresponding source/drain extensions are free from silicide spiking.

[c24] An IC as in claim 23, wherein said source drain/extensions are laterally formed on an angled undercut following a silicon crystal (111) crystallographic plane.

[c25] An IC as in claim 18, wherein said silicide is a silicide of a material selected from a group of materials consisting of a silicide of tungsten (WSi_2), cobalt ($CoSi_2$), nickel (NiSi), titanium (TiSi), platinum (PtSi) and Erbium (ErSi).

[c26] An IC as in claim 25, wherein said silicide is selected from the group of metals consisting of WSi, NiSi and CoSi.

[c27] An IC as in claim 17, wherein said low resistance material layer comprises a metal selected from a group of metals consisting of tungsten, cobalt, nickel, titanium, platinum and Erbium.

[c28] A method of forming an integrated circuit (IC) on a semiconductor substrate, said method comprising the steps of:

a)etching a semiconductor surface in source/drain areas;

b)forming a source/drain extension in etched said source/drain areas;

c)forming a low resistance layer on said semiconductor surface, said low resistance layer forming on each said source/drain extension; and

d)selectively removing vertical portions of said low resistance layer, said low resistance layer being removed from device gate sidewalls and remaining on device gates and each said source/drain extension.

[c29] A method of forming an IC as in claim 28, wherein before the etching step (a) device gates are formed comprising the steps of:

a1)forming a gate dielectric layer on said semiconductor

surface;

a2)depositing a gate material layer on said gate dielectric layer;

a3)patterning said gate material layer and said gate dielectric layer, gates being formed on gate dielectric; and

a4)forming spacers along gate sidewalls, said spacers being less than 100Å thick.

[c30] A method of forming an IC as in claim 28, wherein the semiconductor surface is a silicon surface and the etching step (a) etches into said silicon surface in an angled undercut following a silicon (111) crystallographic plane.

[c31] A method of forming an IC as in claim 28, wherein the semiconductor surface is a silicon surface on an SOI wafer and the etching step (a) etches into said silicon surface to an underlying insulating layer.

[c32] A method of forming an IC as in claim 28, wherein the semiconductor surface is a surface of a silicon wafer and the etching step (a) comprises converting the silicon surface to amorphous silicon and removing said amorphous silicon.

[c33] A method of forming an IC as in claim 32, wherein converting the silicon surface to amorphous silicon comprises implanting a 10^{14} $10^{15}/cm^2$ dose of large ions at

1 50KeV into said silicon surface, said large ions having an atomic number at least that of silicon.

[c34] A method of forming an IC as in claim 33, wherein said large ions are ions of a material selected from the group of materials consisting of arsenic (As+), xenon (Xe+), argon (Ar+), silicon (Si+) and germanium (Ge+).

[c35] A method of forming an IC as in claim 28, wherein forming the source/drain extension in step (c) comprises depositing an in-situ doped silicon layer, forming the in-situ doped silicon layer comprising the steps of:
i)forming a mask over said device regions defined for a first device type;
ii)selectively depositing in-situ doped silicon, doped for a second device type;
iii)forming a mask over said device regions defined for said second device type; and
iv)selectively depositing in-situ doped silicon, doped for said first device type.

[c36] A method of forming an IC as in claim 28, wherein forming the source/drain extension in step (c) comprises the steps of:
i)selectively depositing a first doped oxide on said etched semiconductor surface, doped for a first device type;

ii)selectively depositing a second doped oxide on said etched semiconductor surface, doped for a second device type; and

iii)annealing with a rapid thermal anneal such that lateral junction depth is less than 100Å.

[c37] A method of forming an IC as in claim 28, wherein the low resistance layer is a silicide layer and the step (d) of selectively forming the silicide layer comprises the steps of:

i)forming a silicide layer on said semiconductor substrate;

ii)forming a non conformal masking layer on said silicide layer;

iii)removing portions of said masking layer from vertical silicide layer surfaces; and

iv)removing exposed portions of said silicide layer.

[c38] A method of forming an IC as in claim 37, wherein said silicide layer is deposited using chemical vapor deposition (CVD) to deposit a 50-500Å thick silicide layer at 250 - 500^{o}C.

[c39] A method of forming an IC as in claim 28, wherein the low resistance layer is a metal layer and the step (d) of selectively forming the metal layer comprises the steps of:

i)forming a metal layer on said semiconductor substrate;

ii)forming a non conformal masking layer on said metal layer;

iii)removing portions of said masking layer from vertical metal layer surfaces; and

iv)removing exposed portions of said metal layer.

[c40] A method of forming an IC as in claim 28, further comprising the step of:

f)removing excess said low resistance layer material.